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EXAMINER

SONG, JASMINE

ART UNIT

PAPER NUMBER

2188

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/827,134

Applicant(s)

TALREJA ET AL.

Examiner

Jasmine Song

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 25 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-11, 18 and 19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 18-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **Detailed Action**

1. This office action is in response to Amendment B, mailed 03/25/2004, paper #8, claims 12-17 are previously cancelled, Claims 1-11 and 18-19 are therefore still pending. All rejections and objections not explicitly repeated below are withdrawn.

## **Specification**

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

## **Claim Rejections - 35 USC § 103**

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al., U.S. Patent 5,867,430 and AAPA (Applicant Admitted Prior Art), in view of Alexis et al., U.S. Patent 6,182,189 B1.

Regarding claim 1, AAPA teach that an integrated circuit comprising: a memory array having a first plane, a second plane, a third plane, and a fourth plane (page 1 of the specification, section 0002 lines 5-6), Chen also teaches a memory device is divided into two or more banks which are considered as two or more four planes (col.2, lines 1-2), in addition, Chen teaches that a first partition of the memory array comprises one of the planes (it is taught as the bank receives a write command is considered as the first partition of the memory device, col.2, lines 10-11) and a second partition of the memory array comprises the remaining planes (the rest of banks are accessed by the read operations, col.2, lines 12-14), wherein a write operation is performed on the first partition and a read operation is concurrently performed on the second partition (it is taught as the simultaneous read and write operations in the flash memory device, col.2, lines 12-14);

AAPA and Chen do not teach that a status register coupled to the memory array, wherein the status register provides status information of the first plane, the second plane, the third plane, and the fourth plane. AAPA teaches each partition of the memory array has a designated status register (page one of the specification, section 0003, lines 2-3), Chen teaches a status register of the flash memory device is used to detect the end of the program or erase (write) operation before initiating a read operation to the flash memory device (col.1, lines 28-30).

However, Alexis teaches that a status register coupled to the memory array (Fig.2, status register 150 coupled to the first and second plane which are included in the memory array), wherein the status register provides status information of the first

plane, the second plane, the third plane, and the fourth plane (it is taught as a single status register may be used for both the first and the second planes col.4, lines 3-5, in this case, a single status register can be used for multiple planes since AAPA and Chen teaches four planes or four banks).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Alexis in the flash memory system of Chen or AAPA and have a single status register providing status information for multiple planes or banks because costs is a factor, less circuitry and less cost are needed for a single status register compare to each status register for each memory planes (Chen's reference, co.1, lines 20-51), furthermore, the design of the flash memory device is less complex. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a single status register providing status information for the multiple planes or banks for the advantage stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 6, Chen and AAPA teach that a method of reading while writing to a memory array (col.1, last two lines of Chen and page 1 of specification, section 0002, last three lines), comprising: dividing the memory array into n planes, wherein n is an integer greater than two (page 1 of the specification, section 0002 lines 5-6), Chen

also teaches a memory device is divided into two or more banks which are considered as two or more planes (col.2, lines 1-2); defining a write partition, wherein the write partition is a single plane of the memory array (it is taught as the bank receives a write command is considered as the first partition of the memory device, col.2, lines 10-11), defining a read partition, wherein the read partition is made up of all of the remaining n planes of the memory array (the rest of banks are accessed by the read operations, col.2, lines 12-14);

AAPA and Chen do not teach providing the status of the read partition and the write partition of the memory array with a single status register. AAPA teaches each partition of the memory array has a designated status register (page one of the specification, section 0003, lines 2-3), Chen teaches a status register of the flash memory device is used to detect the end of the program or erase (write) operation before initiating a read operation to the flash memory device (col.1, lines 28-30).

However, Alexis teaches that a status register coupled to the memory array (Fig.2, status register 150 coupled to the first and second plane which are included in the memory array), wherein the status register provides status information of the first plane, the second plane, the third plane, and the fourth plane (it is taught as a single status register may be used for both the first and the second planes col.4, lines 3-5, in this case, a single status register can be used for multiple planes since AAPA and Chen teaches four planes or four banks).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Alexis in the flash memory system of

Chen or AAPA and have a single status register providing status information for the read partition and the write partition of the memory array because costs is a factor, less circuitry and less cost are needed for a single status register compare to each status register for each memory planes (Chen's reference, co.1, lines 20-51), furthermore, the design of the flash memory device is less complex. It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a single status register providing status information for the multiple planes or banks for the advantage stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 2, Chen teaches that the first partition of the memory array comprises the second plane and the second partition of the memory array comprises the first plane, third plane, and the fourth plane (it is taught as the write partition comprises one bank, and the read partition comprises the rest of banks, col.2, lines 10-14, in this case, second read partition comprises multiple banks since Chen teaches four planes or four banks).

Regarding claim 3, Alexis teaches that further comprising:

a microcontroller (col.3, lines 63-67) coupled to the status register, wherein the microcontroller supplies control signals to the status register (Fig.2).

Regarding claim 4, AAPA teaches that the first plane, the second plane, the third plane, and the fourth plane comprise equal memory storage capacities (it is taught as size of 4Mb).

Regarding claim 5, Alexis further teaches an user interface coupled to the status register, wherein the user interface communicates status register information to be used to decide subsequent operations (col.6, lines 1-8).

Regarding claim 7, AAPA teaches the memory array consists of multiple 4 Mb memory planes.

Regarding claim 8, Alexis teaches that the multiple 4 Mb memory planes consist of nonvolatile memory cells (col.1, lines 19-21 and lines 43-45).

Regarding claim 9, Alexis teaches that the nonvolatile memory cell is a flash memory cell (Fig.1 and 2, flash memory 115).

Regarding claim 10, Alexis teaches that the write partition has a dynamic memory address, wherein the memory address changes any time a program or erase

operation begins or resumes in a new memory plane (Fig.3, col.7, lines 38 to col.8, lines 15).

Regarding claim 11, Alexis teaches that if no program or erase operation is performed, the read partition and the write partition are allocated to the same memory location (read-while write operation and col.6, lines 52-60).

5. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al., U.S. Patent 5,867,430, in view of Alexis et al., U.S. Patent 6,260,103 B1.

Regarding claim 18, Chen teaches that an apparatus comprising: means for partitioning a memory array into a fixed first partition (it is taught as the bank receives a write command is considered as the first partition of the memory device, col.2, lines 10-11) and a second partition (another bank is accessed by the read operation, col.2, lines 12-14) to enable multiple operations (reading, and programming, erasing (writing operation) to be performed on the memory array at the same time (col.1, last two lines and col.2, lines 10-12); and means for monitoring the operations performed on the memory array (it is taught as a state machine for monitoring the read and write operations on the memory device, col.2, lines 24-26 and col.11, lines 39-42 and col.5, lines 18-23 and lines 38-50).

Chen does not specifically teach that the second partition is variable even he mentions that the memory device is divided into two or more banks (col.1, lines 28-30).

However, Alexis ('103) teaches a fixed first partition a variable second partition (col.4, lines 20-23).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Alexis in the flash memory system of Chen and employ the fixed partition performing the read operation and the variable second partition performing the write operation in RWW (read-while-write) memory or vice versa in order to reducing instantaneous power consumption for the flash memory and reducing in the amount of additional integrated circuit space (Alex's reference, co.3, lines 21-27). It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a variable second partition for the advantage stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 19, Chen teaches that further comprising a means for communicating the status of the operations performed on the memory array to a user (it is taught as the state machine monitoring the read and write operations and provide status information to the user).

### **Response to applicant's Arguments**

6. Applicant's arguments filed 03/25/2004 regarding independent claims 1,6 have been fully considered but they are not persuasive.

Regarding applicant's arguments of claims 1 and 6 (see applicant's remarks page 5-8), the Examiner notices that the applicant argues the wrong reference, the Examiner applied Alexis' reference US 6182189 in the final rejection (please refer back the final rejection dated on 01/23/2004), **not Alexis US 6260103 B1**.

7. Applicant's arguments with respect to claim 18-19 (regarding the variable second partition) have been considered but are moot in view of the new ground(s) of rejection.

In response to Applicant's argument that Chen does not disclose monitoring the operations performed on a memory array. The Examiner believes this limitation is taught in col.5, lines 18-23 and lines 38-50, the state machine monitors and performs the read and write operations.

8. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

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9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

May 25, 2004

Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100